Claims

[c1] What is claimed is:

1.A grid array (GA) package integrated circuit(IC), the integrated circuit comprising:

a substrate; and

a chip on the substrate, the chip comprising:

a core circuit;

a plurality of I/O devices, each I/O device comprising a plurality of I/O units;

a plurality of bonding pads arranged in a multi-tier structure surrounding said I/O device;

a plurality of traces and a plurality of vias on a plurality of metal layers of the chip for selectively electrically connecting each I/O device and each bonding pad;

a plurality of rings and a plurality of fingers surrounding the chip on the substrate; and

a plurality of bonding wires for electrically connecting each bonding pad to a corresponding finger or to a corresponding ring;

wherein different bonding pads selectively share a same I/O device through the traces.

[c2] 2.The integrated circuit of claim 1 wherein each I/O device comprises four I/O units, and the top-most metal layers form four corresponding metal rings.

[c3] 3.The integrated circuit of claim 2 wherein the four I/O units are a core circuit ground (GND) I/O unit, a core circuit power (V_{DD}) I/O unit, an I/O buffer circuit power (V_{CC}) I/O unit, and an I/O buffer circuit ground (V_{SS}) I/O unit, respectively.

[c4] 4.The integrated circuit of claim 3 wherein the V_{SS} I/O unit in each I/O device forms a top metal ring farthest from the center of the chip.

[c5] 5.The integrated circuit of claim 3 wherein a bonding pad electrically connected to V_{SS} and a bonding pad electrically connected to a signal share one of the I/O devices.

[c6] 6.The integrated circuit of claim 3 wherein a bonding pad electrically connected to V_{SS} and a bonding pad electrically connected to power share one of the I/O devices.

[c7] 7.The integrated circuit of claim 3 wherein a bonding pad electrically connected to V_{SS} and a neighboring bonding pad in a different tier share a same I/O device.

[c8] 8.The integrated circuit of claim 3 wherein a bonding pad electrically connected to V_{SS} and a bonding pad electrically connected to a signal share one of the I/O devices.

[c9] 9.The integrated circuit of claim 3 wherein a bonding pad electrically connected to V_{SS} and a bonding pad electrically connected to power share one of the I/O devices.

[c10] 10.The integrated circuit of claim 3 wherein each bonding pad electrically connected to V_{SS} shares a same I/O device with another bonding pad to minimize the number of I/O devices utilized by the V_{SS} bonding pads.

[c11] 11.The integrated circuit of claim 3 wherein one V_{CC} I/O unit, one V_{DD} I/O unit and one GND I/O unit in three neighboring I/O devices are electrically connected to three bonding pads respectively, and three V_{SS} I/O units in the three neighboring I/O devices are electrically connected to at least one V_{SS} bonding pad to share said neighboring I/O devices.

[c12] 12.The integrated circuit of claim 3 wherein the number of I/O devices occupied exclusively by the V_{SS} I/O units is zero by sharing said I/O devices.

[c13] 13.The integrated circuit of claim 3 wherein the bonding pads electrically connected to the V_{SS} I/O units are situated in the outermost rows of bonding pads.

[c14] 14.The integrated circuit of claim 13 wherein the bonding pads electrically connected to the V_{SS} I/O units are electrically connected to a ground ring through a plurality of bonding wires that each have a shortest path to minimize the total inductance (L) of the bonding wires.

[c15] 15.The integrated circuit of claim 3 wherein the bonding pads electrically connected to the V_{CC} I/O units are situated in the outermost rows of bonding pads.

[c16] 16.The integrated circuit of claim 15 wherein the bonding pads electrically connected to the V_{CC} I/O units are electrically connected to a power ring through a plurality of bonding wires that each have a shortest path to minimize the total inductance (L) of the bonding wires.

[c17] 17.The integrated circuit of claim 1 wherein the bonding pads are arranged in a tri-tier staggered manner.

[c18] 18.The integrated circuit of claim 1 wherein the integrated circuit is a very large scale integrated (VLSI) circuit, or an ultra large scale integrated (ULSI) circuit.